How DSP is Killing Analog in SerDes

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Agenda

- Introductory
- Architecture Comparisons
- Deep Dive I – Linear Equalization
- Deep Dive II – Timing Recovery
- Summary

About the Presenter

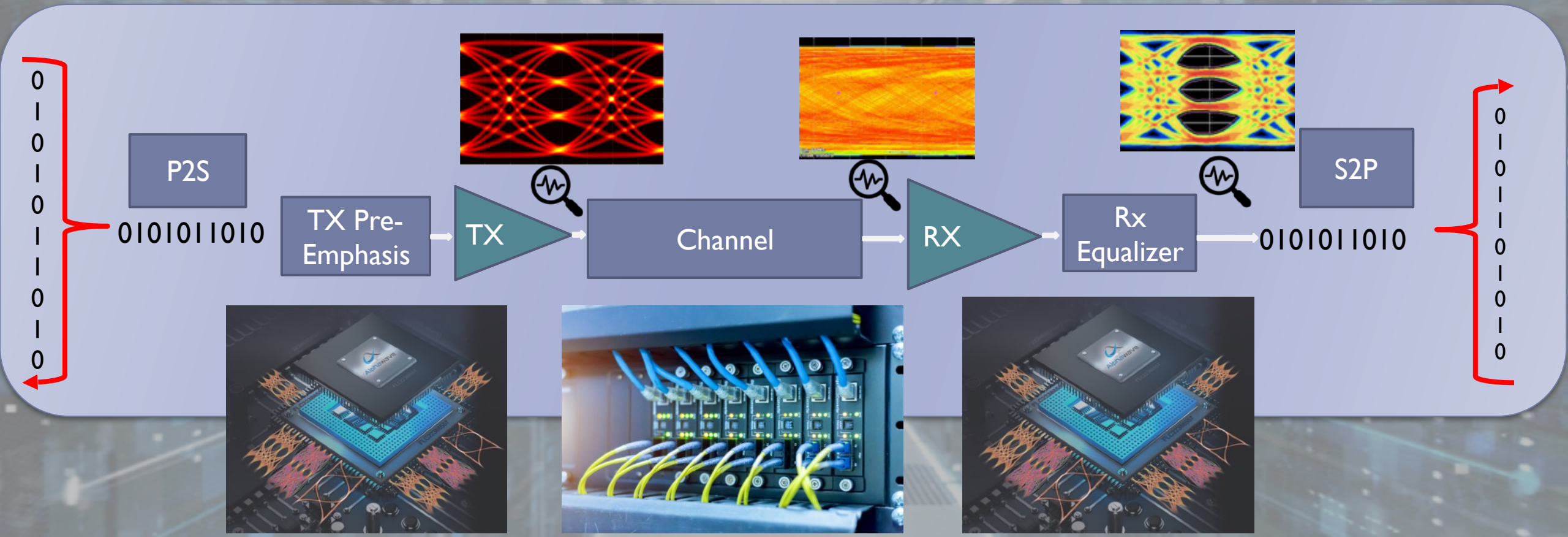
Tony Pialis

President & CEO of Alphawave

Founder of AlphaWave team and visionary in world of Multi-Standard SerDes and Multi-Standard Radio IP technologies

- Former Vice President, Intel Corporation with deep technical and M&A experience
- Founder, V-Semi – Global leader in SerDes IP technology – Acquired by Intel in 2012
- Executive, Snowbush Microelectronics – Leader in SerDes IP technology – Acquired by Gennum in 2007

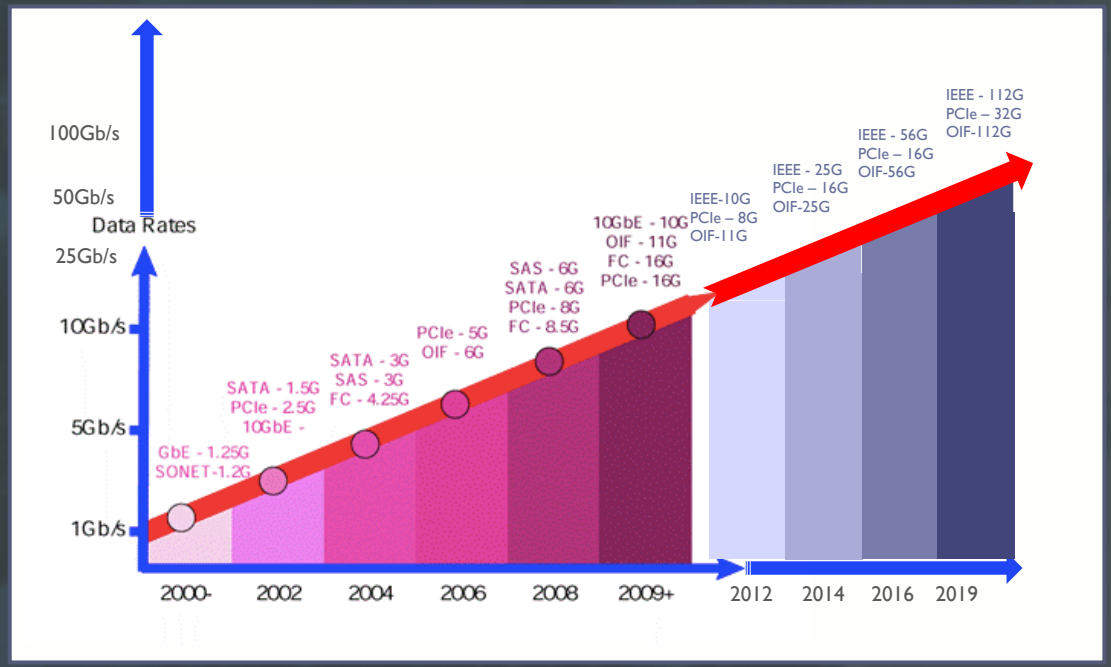
SerDes System Basics



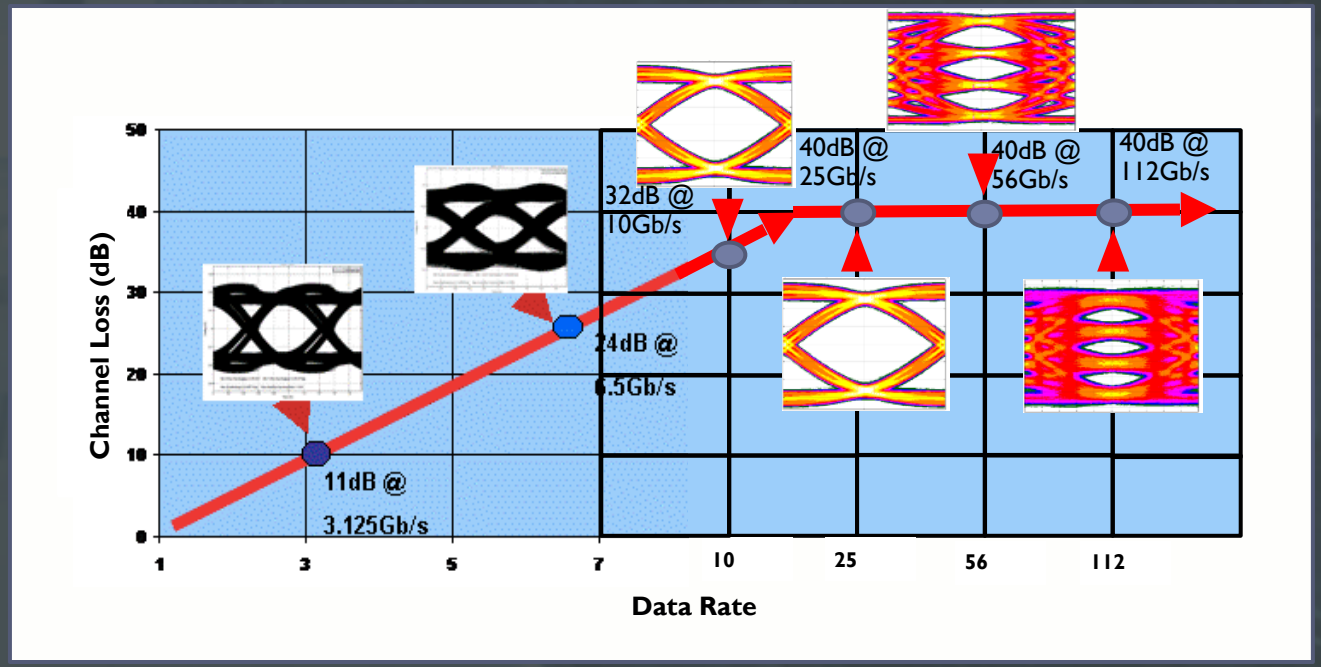
Scaling Data Rates and Losses

Left hand part of diagrams were presented at the 2007 Design and Reuse Conference

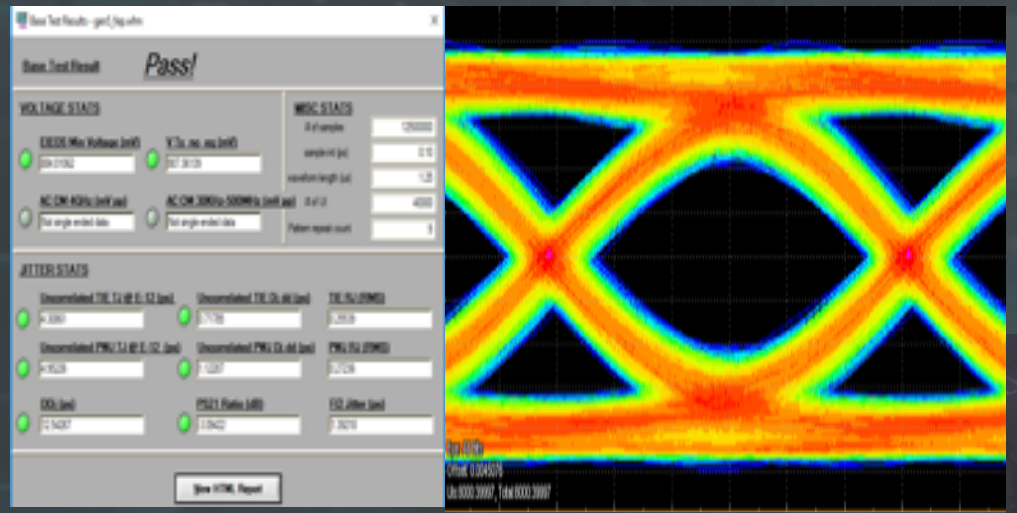
Interface Speeds over Last 20 Years



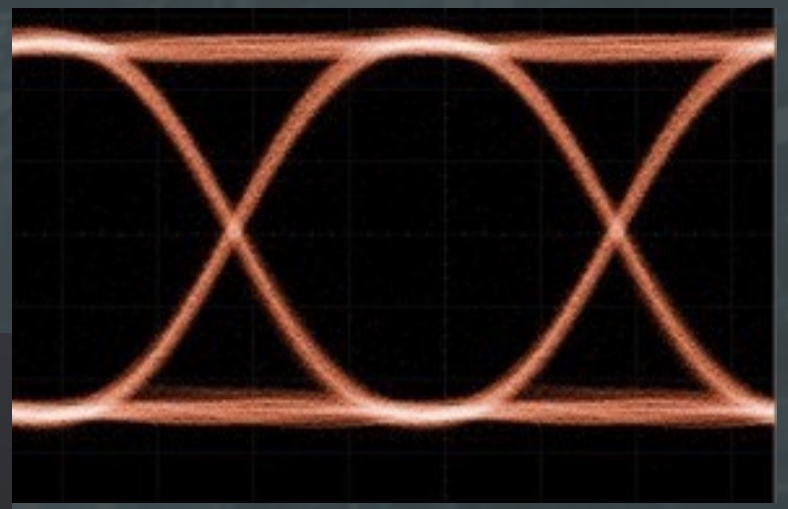
Channel Losses/Modulation Schemes Versus Data Rate



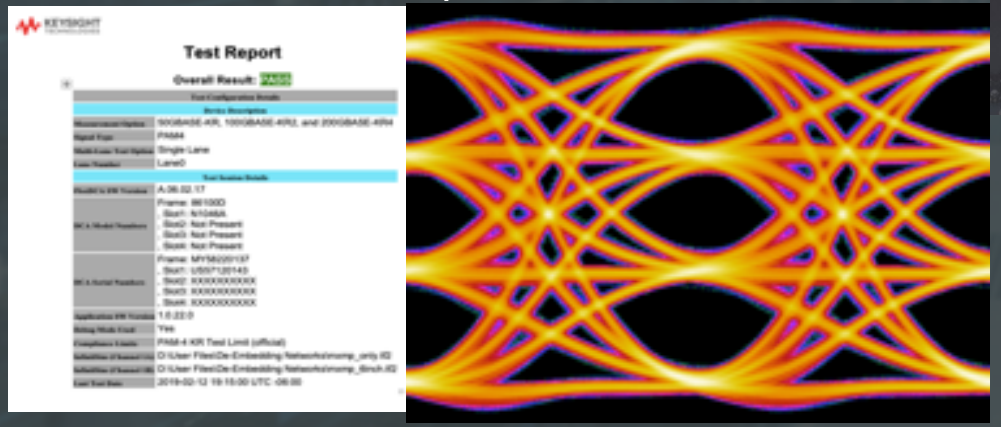
Multi-Standard DSP SerDes is Possible at 100G



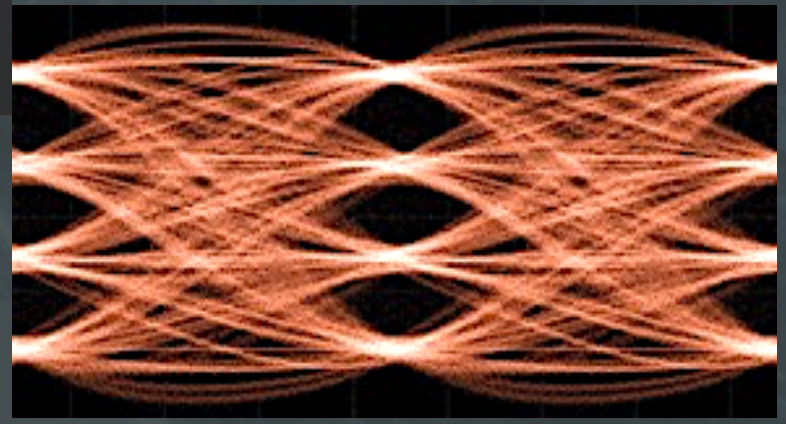
32Gbps PCIe Gen5



25G/28G NRZ - Ethernet



56Gbps PAM4 Ethernet/OIF



112Gbps Ethernet

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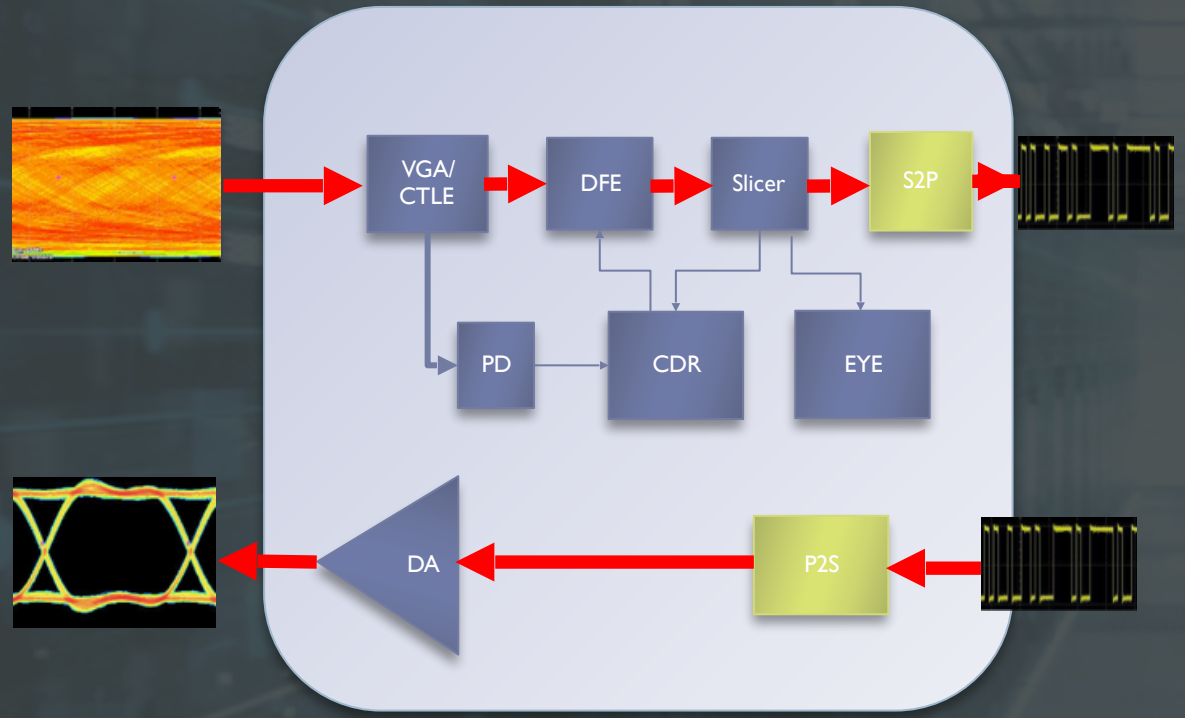
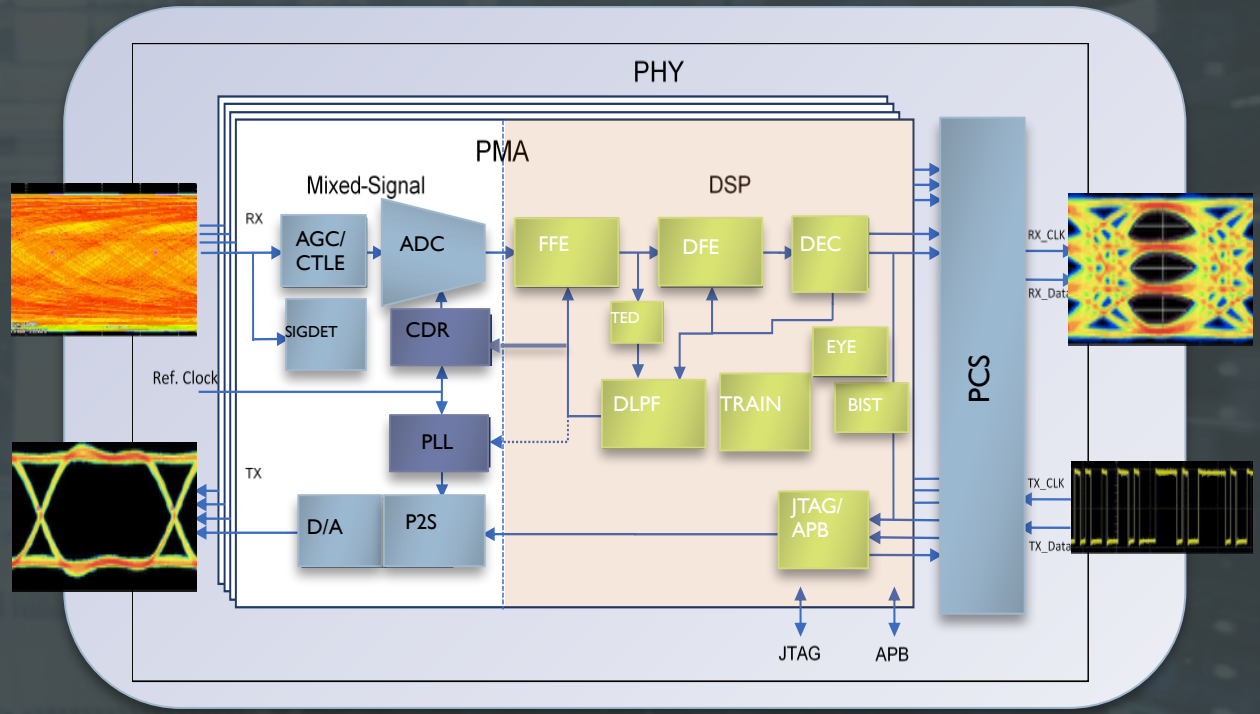
Analog Versus DSP Architectures

Analog SerDes



- Works reliably up to 36dB NRZ / 30dB PAM4
- Analog Eq **sensitive** to process
- Multi-tap Analog DFE is difficult to scale to PAM4
- Lots of DACs/ Comparators

ADC/DSP SerDes



- Works reliably up to 45dB NRZ / 36dB PAM4
- DSP Eq **insensitive** to process
- Challenging ADC
  - Up to 56GSps
- Simplified DSP based training

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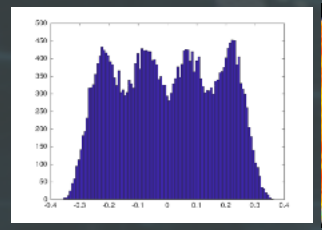
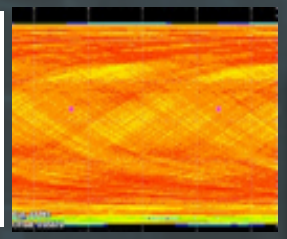
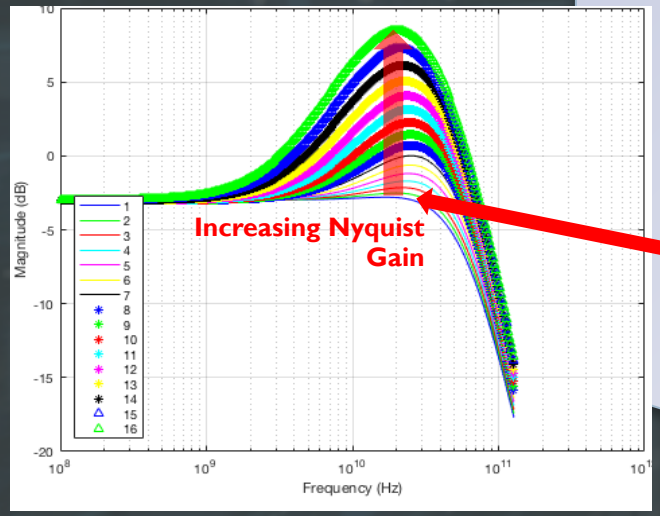
Analog Linear Equalization

Analog CTLE / VGA Architecture Example

Pre-Trained Signal Constellation

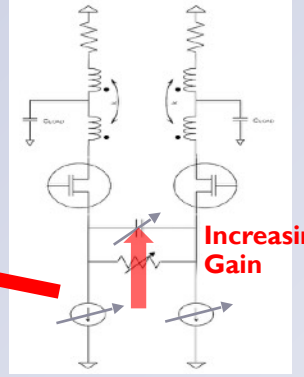


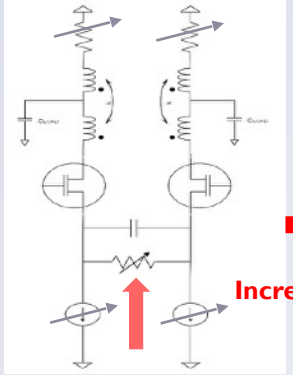




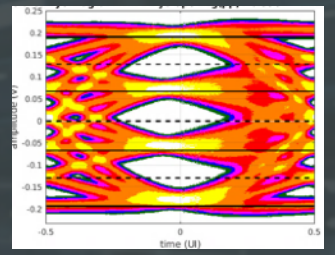
CTLE/VGA Stage1

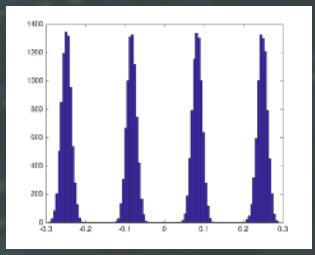
CTLE/VGA Stage2

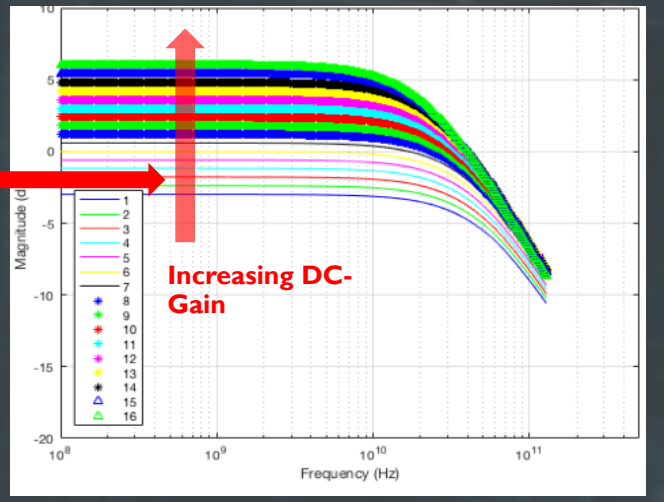




Post-Trained Signal Constellation



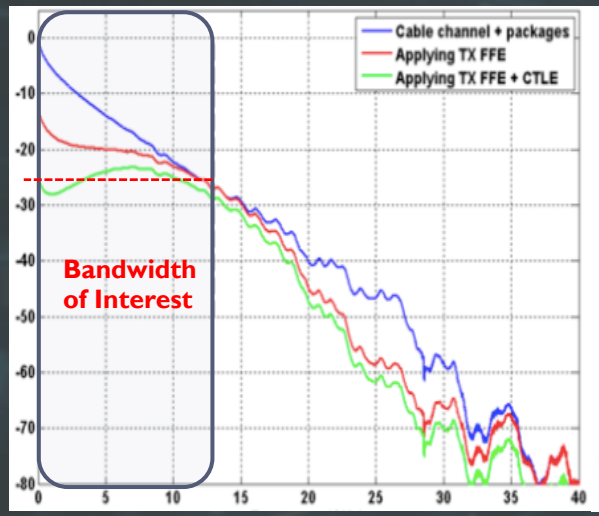




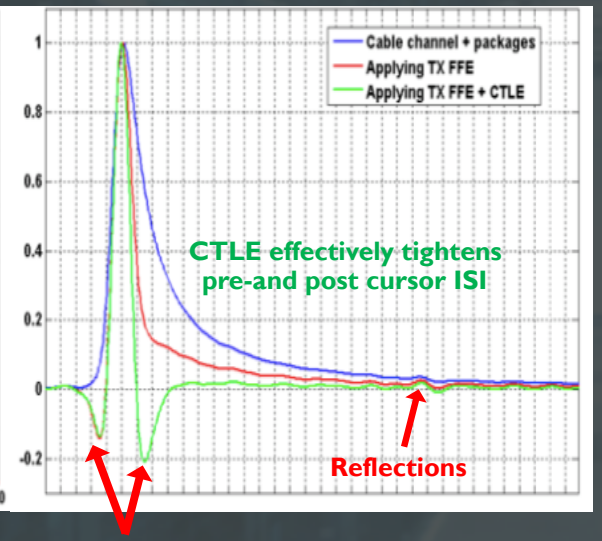
Analog Strengths & Weaknesses

Analog CTLE / VGA Challenges

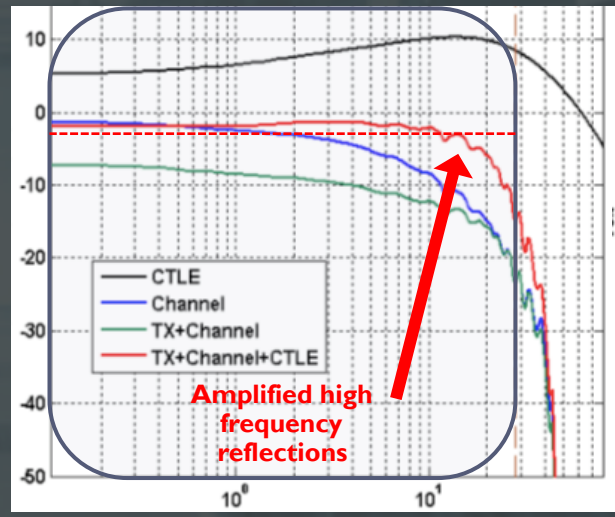
- Building a tunable CTLE that can optimally flatten backplanes, cables and connectors is virtually impossible

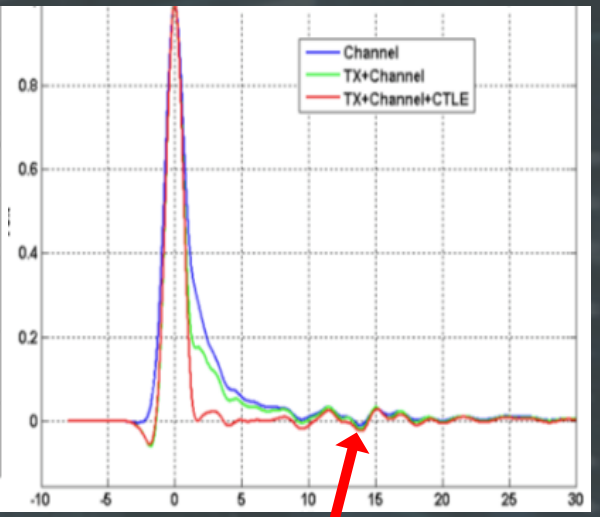


- Try to flatten out channel response with TX FIR + CTLE



- Non-flatness of channel response create pre and post overshoot in pulse response





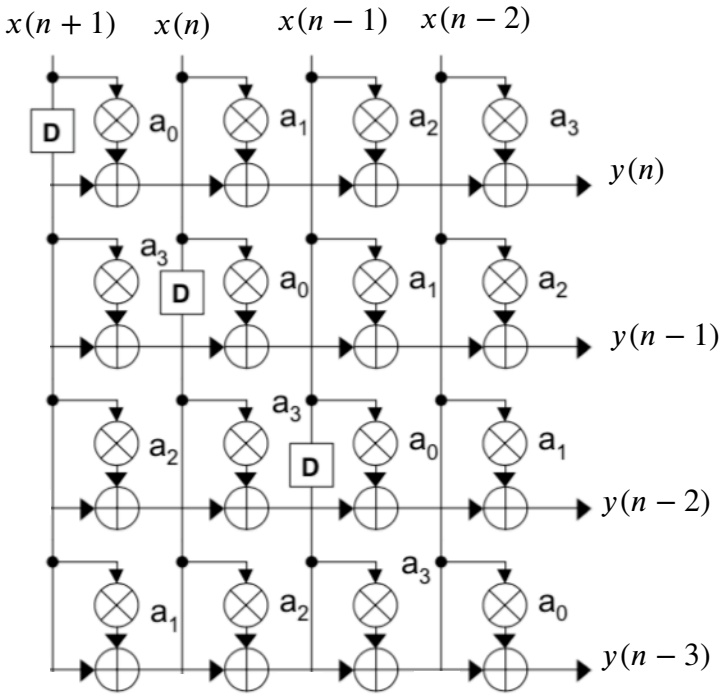
- Amplification of channel loss also amplifies destructive high frequency reflections

DSP: Linear Equalization

Digital RX FIR Filter

- By quantizing an analog signal, we can use a digital FIR filter to approximate any desired complex frequency response

Block DSP FIR Filter (4x4): 4bytes/block x 4tap FIR



Parallel FIR filters are needed to reduce clock speeds to reasonable rates (< 1GHz)

$$|TF(DC)| = \sum_{i=0}^{N} a_i$$

$$|TF(Nyquist)| = \sum_{i=0}^{N} a_i - a_{i-1}$$

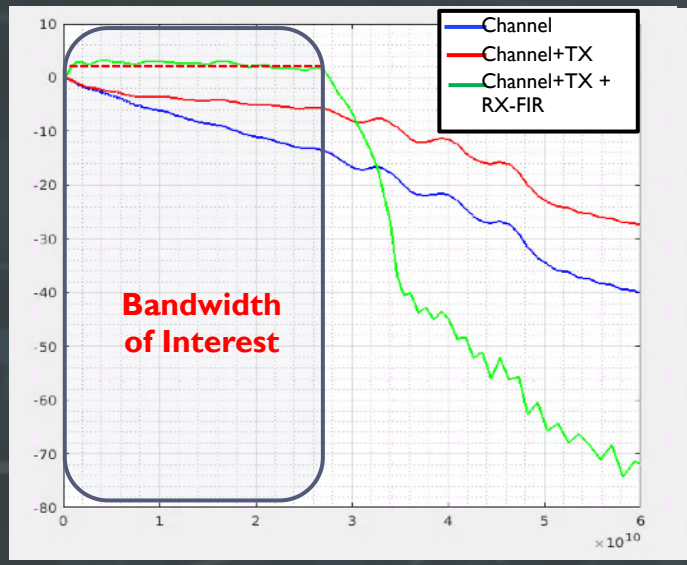
$$\left|TF\left(\frac{Nyquist}{2}\right)\right| = \sqrt{\left(\sum_{i=0}^{N} a_i \cdot \sin\left(\mathrm{i} \cdot \frac{\pi}{4}\right)\right)^2 + \left(\sum_{i=0}^{N} a_i \cdot cos\left(\mathrm{i} \cdot \frac{\pi}{4}\right)\right)^2}$$

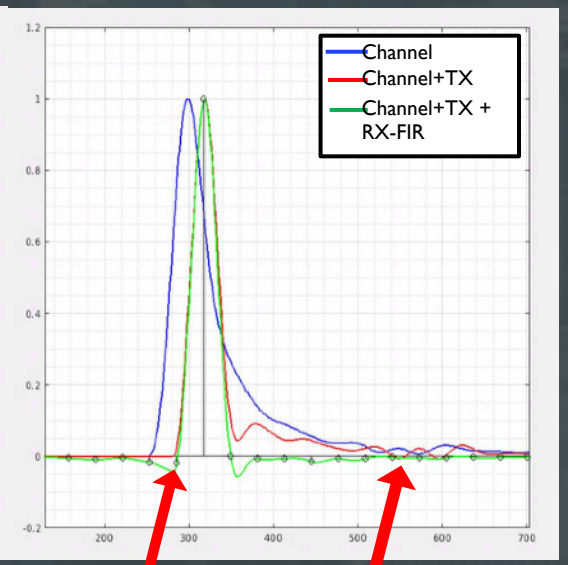
Coefficient range and resolution can be tapered

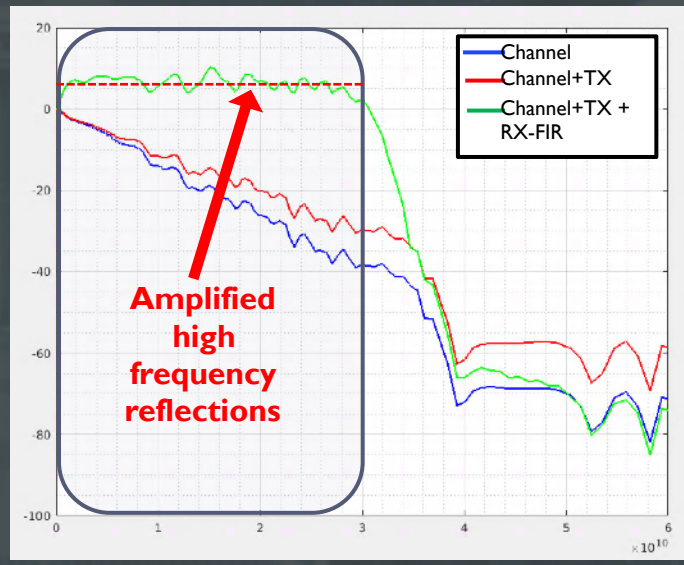
DSP Filtering Strengths & Weaknesses

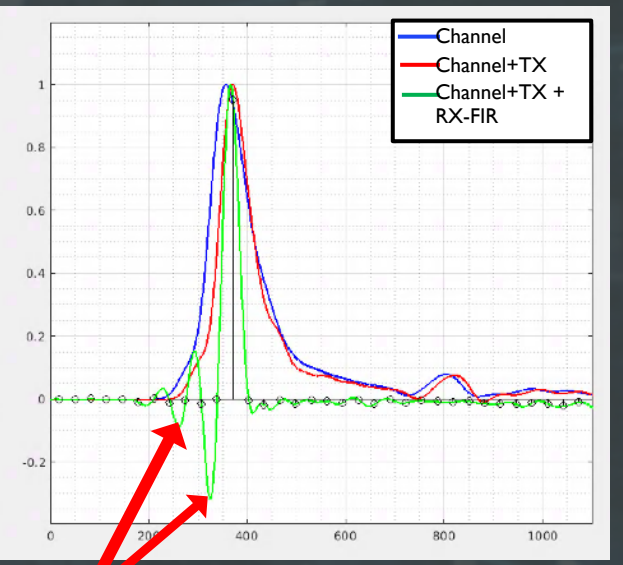
DSP Filtering Strengths

- A multi-tap RX-FIR (eg 5-25 taps) can optimally flatten backplanes, cables, connectors via different sets of FIR coefficients









- RX-FIR effectively flattens our channel response in bandwidth of interest
- Pulse response (pre and post) is optimally equalized using multi-tap RX-FIR
- FFE Solution ensures there is no residual Inter-Symbol Interference at ideal sampling points of the ADC

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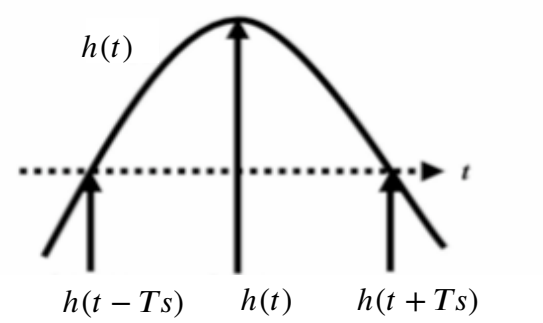
Analog Timing Recovery

High Speed Analog Timing Error Detectors (TED)

- Baud rate sampling is most popular at high speeds – Mueller-Muller (MM) and Minimal Mean Squared Error (MMSE)

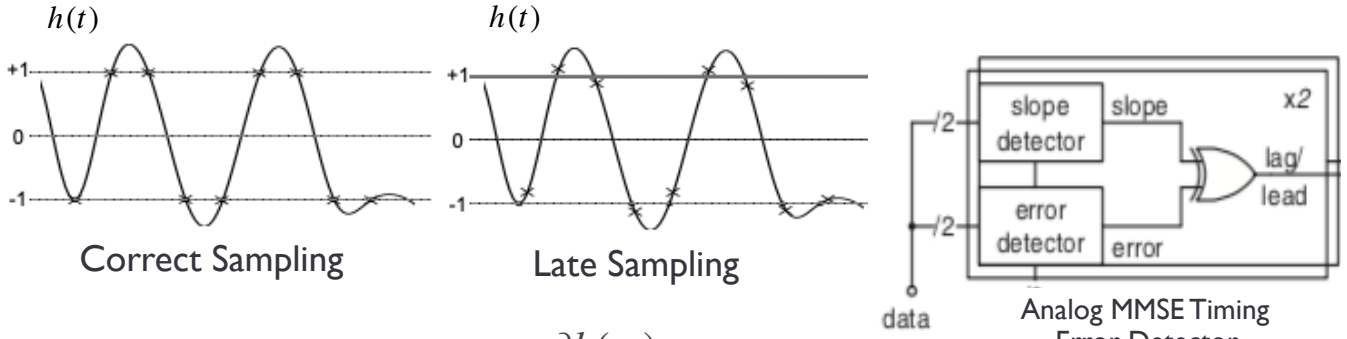
Mueller-Muller Timing Error Detector



- MM-ClassA: $h(t - Ts) = h(t + Ts)$
- MM-ClassB: $h(t - Ts) = 0$

- Quarter rate PAM4 analog receivers require more than 20 comparators to implement – high power

MMSE Timing Error Detector



$$TED_{OUT} = Err(\tau_0) \bullet \frac{\partial h(\tau_0)}{\partial \tau_0}$$

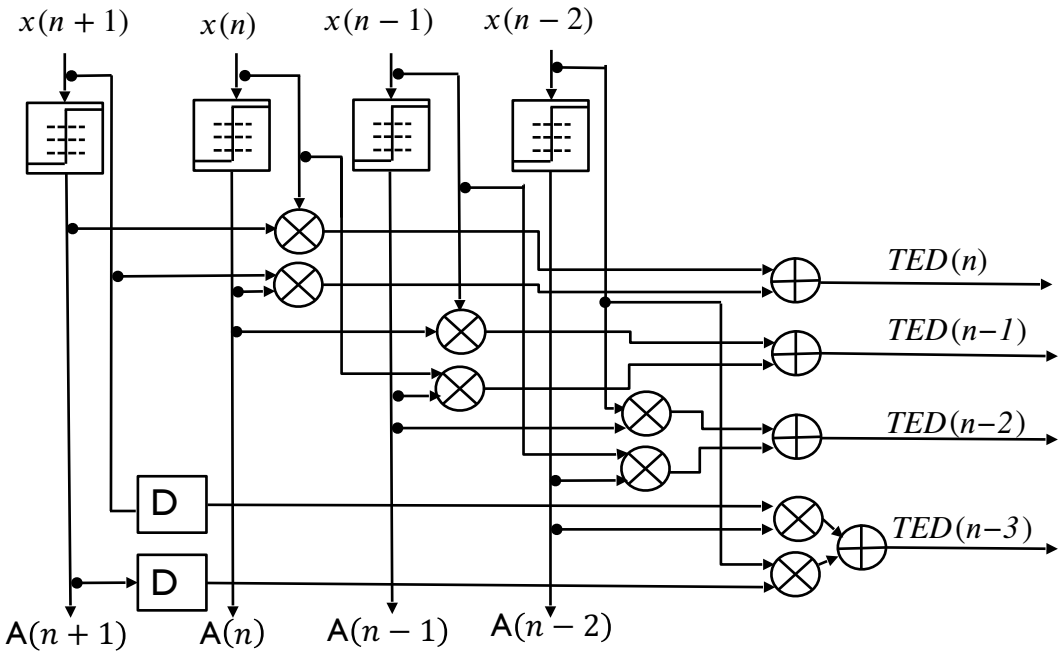
- Requires sub-baud rate sampling for slope detector
- Very power intensive at high speeds
-

DSP: Timing Recovery

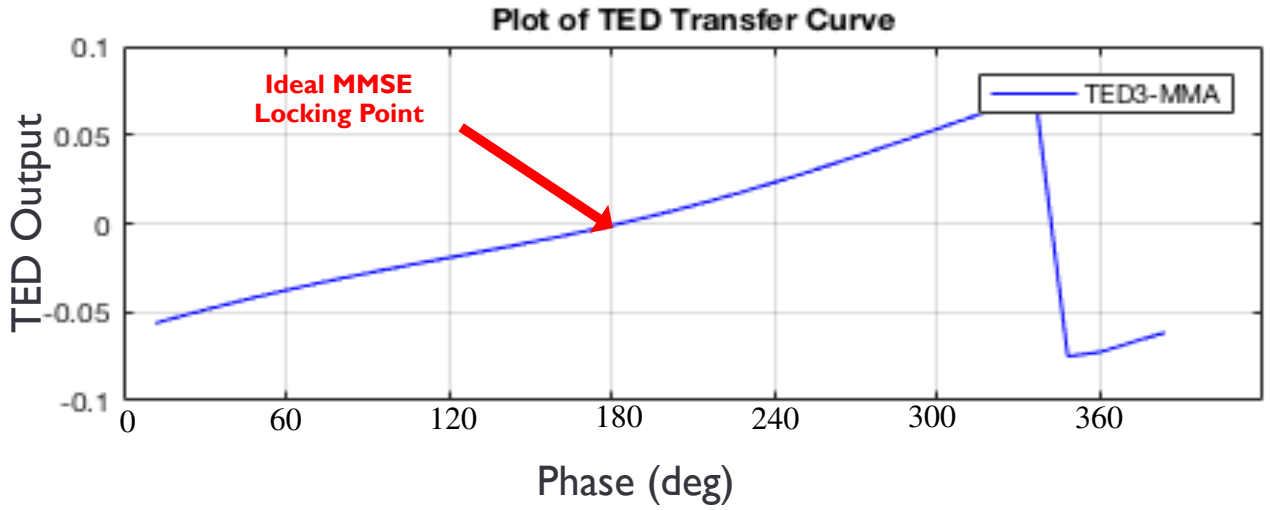
High Speed Digital Timing Error Detectors

- Mueller-Muller (MM) Class-A / Class-B approaches can be applied directly to quantized (ADC) signals

Block DSP (4x4) Mueller-Muller Class A Timing Error Detector



- Digital TED enables linearized CDR operation
- For PAM4, only specific transitions are used (eg. +1/-1)
- Separate frequency acquisition circuit is needed for +/-5000ppm



DSP: Timing Recovery

High Speed Digital Timing Error Detectors

- Minimal Mean Squared Error (MMSE) approaches can be applied directly to quantized (ADC) signals

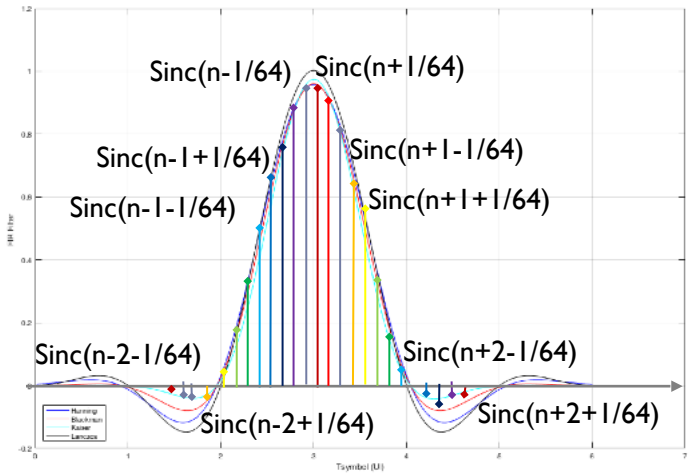
DSP MMSE Timing Error Detectors

- For a bandlimited signal, () a derivative of a sampled signal can be generated by a baud rate FIR based on polyphase Fractional Delay Filter (FDF):

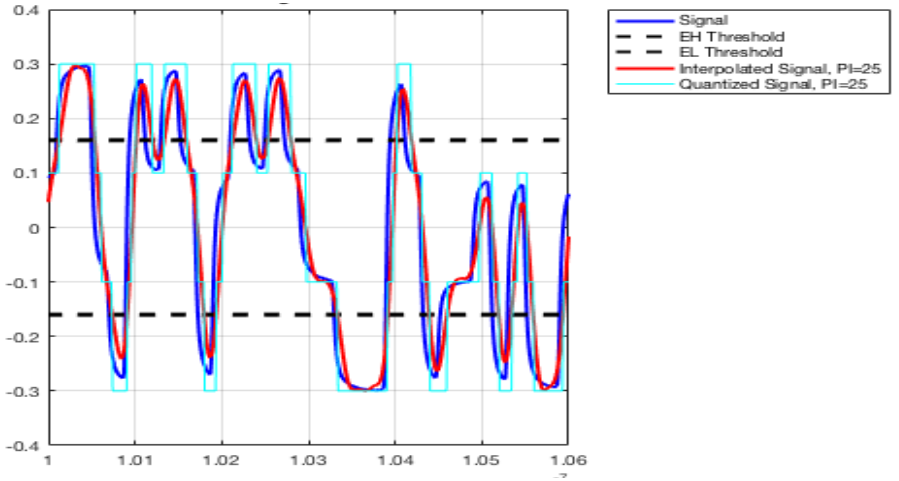
$$\sum_k r(kT)\left[\frac{\cos \pi(t-kT)/T}{(t-kT)} - \frac{\sin \pi(t-kT)/T}{\pi(t-kT)^2/T}\right].$$

Pre-calculate coefficients to implement via single derivative FIR filter

Fractional Delay Filter Pulse Response



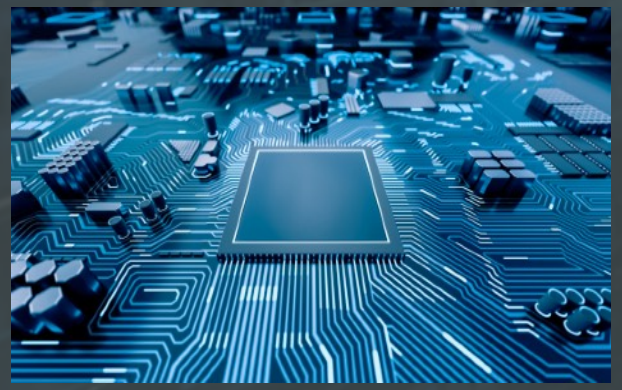
Fractional Delay Filter Time Response

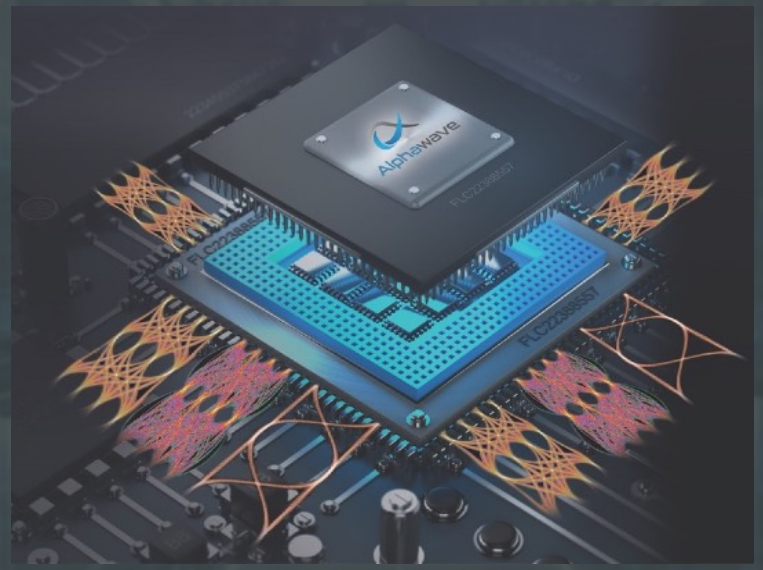


AlphaCORE DSP-based SerDes architecture

Datacenter / AI

Compute / SSD
- PCIe





DSP enables AlphaWave to have the leading Multi-Standard 1-112Gbps Silicon solution available in 7nm

Telecomm / Optical

5G Base Station

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Is the Analog SerDes dying?

Is Analog Finally Dying?

- The use of Analog in SerDes is transitioning to how it is used in RF, read channel, DSL, …
  - Analog is used to drive signals to the outside world
  - Analog is used to quantize real-world incoming signals
  - **Analog is not used to process, or condition signals**
    - **There will be some caveats**
    - **There will always be need for analog designers**
  - What's next for SerDes…
    - The Modem ?